

POWER SAVING METHOD AND ARRANGEMENT FOR A RECONFIGURABLE ARRAY

BACKGROUND OF THE INVENTION

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The present invention relates generally to computer processors. More specifically, the present invention relates to power savings with an array structure of processor cells.

A processing cell contains logic elements for executing an operation on 10 data according to an instruction. Increasingly, larger numbers of processing cells are connected together in one processor to accomplish a greater number of more complex processing tasks. For instance, a processor having cells that are arranged in an array of M rows and N columns is capable of processing $M \times N$ operations during each clock cycle. Further, each cell in the array can be individually programmed to perform a 15 unique operation, such that the processor could accomplish $M \times N$ different operations during a single clock cycle.

In digital systems, dynamic power consumption dominates a system's overall power consumption. Each cell consumes dynamic power in two ways: when 20 its input is changing, and when its internal registers are clocked. Some processing applications require only a portion of the number of cells in a processor to execute a particular function. However, a cell that is not being used for a certain application will still consume dynamic power by having its registers continually clocked while it awaits 25 to be enabled.

Some uses for processors, such as in a handheld computing device or 30 wireless communication device for example, benefit from reduced power consumption. Reduced power consumption allows for a smaller power supply, and thus a more efficient design of such devices. Also, a device with reduced processor power consumption can achieve a longer battery life. Accordingly, there exists a need for a method and arrangement for saving power in a processor.

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SUMMARY OF THE INVENTION

This invention relates to processing architectures and methods of controlling processing cells. In an embodiment of the invention, an MxN array of processor cells includes control and logic circuitry for dynamic reconfiguration of individual cells, whereby a subset of cells is masked and enabled and the remaining unmasked cells are disabled. The enabled cells are activated to accomplish a processing application, and the disabled cells do not consume dynamic power. In this manner, power consumption for the array is reduced, depending on the application.

This invention, embodied as a method, includes the steps of providing a row mask signal configured to enable selected cells in each row of the array, and providing a column mask signal configured to enable selected cells in each column of the array. The method further includes the step of gating the row mask signal and column mask signal with a clock signal of each cell to activate, at the next clock cycle, the enabled cells in the array based on the row mask signal and column mask signal.

In another embodiment of the invention, a method for saving power in an MxN array of processor cells, wherein each cell is configured to execute a context instruction when active, includes masking the array to enable a subset of cells of the array, activating each enabled cell to execute the context instruction, and disabling each unmasked cell in the array, such that each disabled cell does not consume dynamic power.

In yet another embodiment of the invention, a power-saving arrangement for an MxN array of processor cells includes a row mask register configured to provide a row mask signal for enabling selected cells in each row of the array, and a column mask register configured to provide a column mask signal for enabling selected cells in each column of the array. The arrangement also includes a clock circuit, connected to supply each cell with a clock signal, each clock signal being gated with the row mask signal and column mask signal to activate the enabled cells upon a new clock cycle.

In still yet another embodiment of the invention, a power saving arrangement for an MxN array of processor cells includes a mask circuit for generating

a mask signal for masking a portion of the cells in the array, and a clock for providing a clock signal, the clock signal being gated with the mask signal to activate the masked cells upon a new clock cycle.

Selectively enabling and disabling cells in the array configures the array
5 for a particular processing application, yet reduces power consumption depending on the application by powering only enabled and activated cells, and preventing dynamic power from being consumed by disabled cells.

BRIEF DESCRIPTION OF THE DRAWING

10 FIG. 1 shows a dynamically reconfigurable processing architecture including an MxN array of reconfigurable cells.

FIG. 2 depicts an MxN array of reconfigurable cells with enable registers.

15 FIG. 3 illustrates an internal structure of one reconfigurable cell according to an embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

As described above, power consumption by an array of processor cells can be inefficiently large. Even while a particular cell is not actively processing data,
20 the cell may still have its registers clocked and/or inputs changing. Reducing power consumption by a processor is an important goal toward achieving smaller power supplies, both physically and electrically for the processor. In such a case, the processor's utility in certain applications is enhanced.

FIG. 1 shows a dynamically reconfigurable processing structure 100
25 suitable for use with embodiments of the invention. The processing structure 100 includes an M row x N column array of reconfigurable cells 110. In one embodiment, the MxN array is an 8x8 array of cells 110. Each cell 110 includes reconfigurable processing and logic elements which, when programmed, execute one or more logical functions. Each row M is connected to a row context memory 120. The row context
30 memory 120 provides the configuration data to instruct all cells 110 in each row.

Each column N is connected to a column context memory 130. The column context memory is configured to provide instructions to all cells 110 in each column. Thus, a row context from the row context memory 120 is gated with a column context from the column context memory 130 at each cell 110, to address and instruct the particular cell 110.

FIG. 2 shows a processor array 200 with an arrangement for reducing power consumption in the array, according to an embodiment of the invention. An M-bit row mask register 310 is connected to the cells 110 in each row of the MxN array. An N-bit column mask register 320 is connected to the cells 110 in each column of the MxN array. A M-bit word from the row mask register is combined with an N-bit word from the column mask register to mask a portion of the cells in the array 200.

The masked portion of cells is enabled for operation, while the remaining unmasked cells are disabled. The disabled cells are effectively switched off and do not consume dynamic power while the masked cells are activated and operate. The mask can be updated at each cycle, if needed. For a particular cell to be enabled, both corresponding bit lines from the row and column mask registers 210 and 220 must carry a logically active signal, such as a logical "1" for example, depending on a desired convention. Thus, by individually reconfiguring cells, including enabling or disabling cells or a subset of cells of the array, power savings is achieved according to the specific application at hand accomplished by the masked and active cells.

FIG. 3 illustrates the internal structure of one cell 110. In an embodiment, the cell 110 includes one or more functional units 310, 320 and 330. While cell 100 is shown as having three functional units, the number of functional units is merely exemplary, and those having skill in the art would recognize that any combination of functional units can be used within the teachings of the present invention. A combination of active functional units 310, 320 and/or 330 defines an operation of the cell, and represents a logical function executed by the cell 110 during a processing cycle. Suitable functional units can include, without limitation, a Multiply-and-Accumulate (MAC) functional unit, an arithmetic unit, and a logic unit. Other types of functional units for performing functions are possible. The functional

units 310, 320 and/or 330 are configured within the cell 110 in a modular fashion, in which functional units can be added or removed without needing to reconfigure the entire cell 110. In particular, by adding functional units, a range of operations of the cell 110 is expandable and scalable. The modular design of the exemplary embodiment
5 also makes decoding of the function easier.

The functional units are controlled and activated by a context register 340. The context register 340 latches a context instruction from the row context memory or the column context memory upon each processing cycle, and provides the configuration data to the appropriate functional unit(s). Depending upon the structure
10 and logic of the group of functional units, and based on the context of the cell, more than one functional unit can be activated at a time.

Each cell 110 contains a storage register 312 for temporarily storing the functional unit computation results. In one embodiment, the results from each functional unit multiplexed together by multiplexer 304, outputted to a shifter 306, and
15 provided to an output register 316. The data output of the shifter 306 is also provided to the storage register 312, where it is temporarily stored until replaced by a new set of output data from the functional units 310, 320 and/or 330. The output register 316 sends the output data to an output multiplexer 318, from which the output data,
representing a processing result of the reconfigurable cell, is sent to either the data
20 bus, to a neighboring cell, or both.

A row mask signal and a column mask signal are gated with a clock signal at AND gate 303, for controlling all of the sequential logic elements within the cell 110. The row mask signal and the column mask signal is gated at AND gate 307, for activating transition barriers 311, 321, and 331, which in turn prevent input
25 changes from propagating to the internal components. At the same time, all the clocks to the registers, including the context register 340, are disabled. As a result, no dynamic power is consumed in the cell and the cell does not process any data. The row mask signal and the column signal thus control the flow of data to be operated upon by the cell 110.

The row mask signal and the column mask signal are provided by the row and column mask registers 210 and 220, respectively as shown in FIG. 2. By selectively enabling a subset of cells 110 in the array, it is possible to scale the amount of power consumed, such that the consumption of power can be controlled,
5 particularly when needed, such as in the power scarcity, etc.

The reconfigurable cells in an array are interconnected according to one or more hierarchical schemes. In one exemplary embodiment, for an 8x8 array for example, cells within a quadrant, i.e. each group of 4x4 cells, are fully connected in a row or column. Further, cells in adjacent quadrants are connected via specially-
10 configured fast lanes that enable a cell in one quadrant to broadcast function results to all cells in an adjacent quadrant. Thus, the subset of cells that are masked and enabled may follow some hierarchical scheme, or can be randomly or programmatically enabled.

Other embodiments, combinations and modifications of this invention
15 will occur readily to those of ordinary skill in the art in view of these teachings. Therefore, this invention is to be limited only by the following claims, which include all such embodiments and modifications when viewed in conjunction with the above specification and accompanying drawings.

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WHAT IS CLAIMED IS: